Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device utilizing an oscillator installed outside and having an inverting amplifier, which is installed in parallel with the oscillator, ~~that~~ the oscillator intermittently ~~outputs~~ outputting an oscillation signal in response to a ~~given~~ control signal, the inverting amplifier comprising:

a first terminal that receives a first signal from the oscillator;

a second terminal that provides a second signal to the oscillator;

a transmission gate ~~installed~~ disposed between the first terminal and the second terminal, that is formed by using insulated gate transistors, the transmission gate being set to an 'on' state where the first signal is transmitted in a case of the control signal being set to a first logical level, and set to an 'off' state where the first signal is not transmitted in the other case of the control signal being set to a second logical level;

an inverter ~~installed~~ disposed between an output terminal of the transmission gate and the second terminal, that is formed by using the insulated gate transistors, and inverting a logical level of a given signal so as to output the second signal; and

a clamping circuit ~~installed~~ disposed between the output terminal of the transmission gate and an input terminal of the inverter that is formed by using the insulated gate transistor, the clamping circuit being set to make the first signal output from the transmission gate applied to the input terminal of the inverter in a case of the control signal being set to the first logical level, and set to make predetermined voltage applied to ~~the~~ an input terminal of the inverter in the other case of the control signal being set to the second logical level.

2. (Currently Amended) The semiconductor device ~~claimed~~ recited in claim 1, the transmission gate being a CMOS transmission gate, a combination of n-channel type MOS transistors and p-channel type MOS transistors.

3. (Currently Amended) The semiconductor device ~~claimed~~ recited in claim 1, further comprising:

a buffer, that is formed by using the insulated gate transistors, and that the signal output from the inverting amplifier to other circuits.

4. (Currently Amended) The semiconductor device ~~claimed~~ recited in claim 3, further comprising:

a transmission gate that is ~~installed~~ disposed between the inverting amplifier and the buffer, and that is formed by using the insulated gate transistors.

5. (Currently Amended) The semiconductor device utilizing an oscillator ~~claimed~~ recited in claim 1, further comprising:

a feedback resistor that is ~~installed~~ disposed in parallel with the oscillator.

6. (Currently Amended) An oscillation circuit, comprising:

an oscillator; and

a semiconductor device utilizing the oscillator,

the semiconductor device, comprising:

an inverting amplifier, that is ~~installed~~ disposed in parallel with the oscillator, and that intermittently outputs an oscillation signal in response to a given control signal; and

the inverting amplifier, comprising:

a first terminal that receives a first signal from the oscillator;

a second terminal that provides a second signal to the oscillator;

a transmission gate ~~installed~~ disposed between the first terminal and the second terminal~~,~~ that is formed by using insulated gate transistors, the transmission gate

being set to an 'on' state where the first signal is transmitted in a case of the control signal being set to a first logical level, and set to an 'off' state where the first signal is not transmitted in the other case of the control signal being set to a second logical level;

an inverter ~~installed~~ disposed between an output terminal of the transmission gate and the second terminal, that is formed by using the insulated gate transistors, and that inverts a logical level of a given signal so as to output the second signal; and

a clamping circuit ~~installed~~ disposed between the output terminal of the transmission gate and an input terminal of the inverter, that is formed by using the insulated gate transistor, that is set to make the first signal output from the transmission gate applied to ~~the~~ an input terminal of the inverter in a case of the control signal being set to the first logical level, and that is set to make predetermined voltage applied to the input terminal of the inverter in the other case of the control signal being set to the second logical level.